REMARKS

Claims 23 and 24 are cancelled , hence, claims 1-4, 9-15 and 20-22 are all the claims pending in the application.

Claims 1 and 12 are amended.

Applicant thanks the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119, and receipt of the priority documents.

Also, Applicant thanks the Examiner to acknowledging the drawings filed on July 7, 2003.

Claim Rejection 35 U.S.C. § 112

Claims 1 and 12 have been amended that deletes "a data word", therefore the rejection is moot.

Claim Rejections - 35 U.S.C. § 103

Claims 1-4, 9-15 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (EP 0817053 Al, hereinafter "Williams") in further view of Prabhu (US 2003/0056062). Applicant respectfully traverses these rejections because Prabhu fails to disclose or suggest all of the claim limitations. Specifically, the references fail to disclose or suggest at least the following limitations:

Claims 1 and 12:

wherein said monitor element **is connected to a bus which is directly connected to a processor of said first and second computer elements**;

wherein said monitor element **receives address strobes from said processor** during the same cycle in order to determine whether said first computer element is out of said synchronism

Claim 1, as amended, discloses that a monitor element **is connected to a bus *which* is directly connected to a processor of the first and second computer elements**, and **receives address strobes from the processor during the same cycle in order to determine whether the first computer element is out of the synchronism**. Thus, the monitor element is able to receive address strobes from the processor, because the monitor element is connected to the bus which is directly connected to a processor of the first and second computer. Further, the monitor element receives address strobes as soon as the processor outputs them. Furthermore, it is possible to determine whether the first computer element is out of the synchronism as soon as the processor outputs address strobes. As a result, the monitor element detects an out of synchronism early, and accordingly a first computer recovers from the out of synchronism at an early stage.

In contrast, the Examiner concedes that Williams and Prabhu does not teach the information processing apparatus wherein said monitor element receives address strobes (Office Action page 11).

To overcome the above deficiency of Williams, the Examiner cites to Phelps, which allegedly discloses the memory subsystem including an error detection mechanism for address and control signal wherein accessing a location in a DRAM requires an address be applied to the address inputs and the error detection circuit generates new error detection information dependent

upon the address and command information received with each request (Office Action page 11). Phelps discloses that the error detection circuit 130 within the memory module 100 (Fig 3, Col. 1, line 67 and Col. 2 line 1) detects the error based upon the error detection information which is provided by the error detection generation circuit 32 (Col. 3, lines 48-60, and Col. 4, lines 60-67). However, Phelps does not teach or suggest the mechanism for detecting the out of synchronism among a plurality of apparatuses. Moreover, Phelps clearly concedes that the error detection circuit 130 detects errors at last when the error detection *information* arrives at the memory module 100, because the error detection circuit 130 within the memory module 130 detects the error (Fig. 3). Further, the error detection circuit 130 detects errors **after** the processor 20 outputs the memory requests to the memory controller 30 and then the memory controller 30 transfer the memory requests to the memory module 100 (Col. 4, lines 60-67). Furthermore, there is no teaching or suggestion to form the error detection mechanism which detects errors as soon as the processor outputs memory requests (address strobes). Thus, Phelps either alone or in combination with Williams and Prabhu does not teach or suggest the claim limitation of wherein said monitor element receives address strobes.

Therefore, at least for these reasons, Applicant respectfully submits that Claims 1 and 13 are patentable and requests the Examiner to withdraw the rejection..

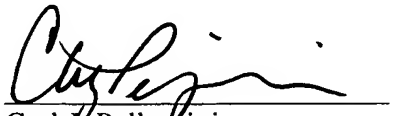
Additionally, claims 2-4, 9-11, 13-15, and 20-22 are allowable at least based on their dependency from claims 1 and 12.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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